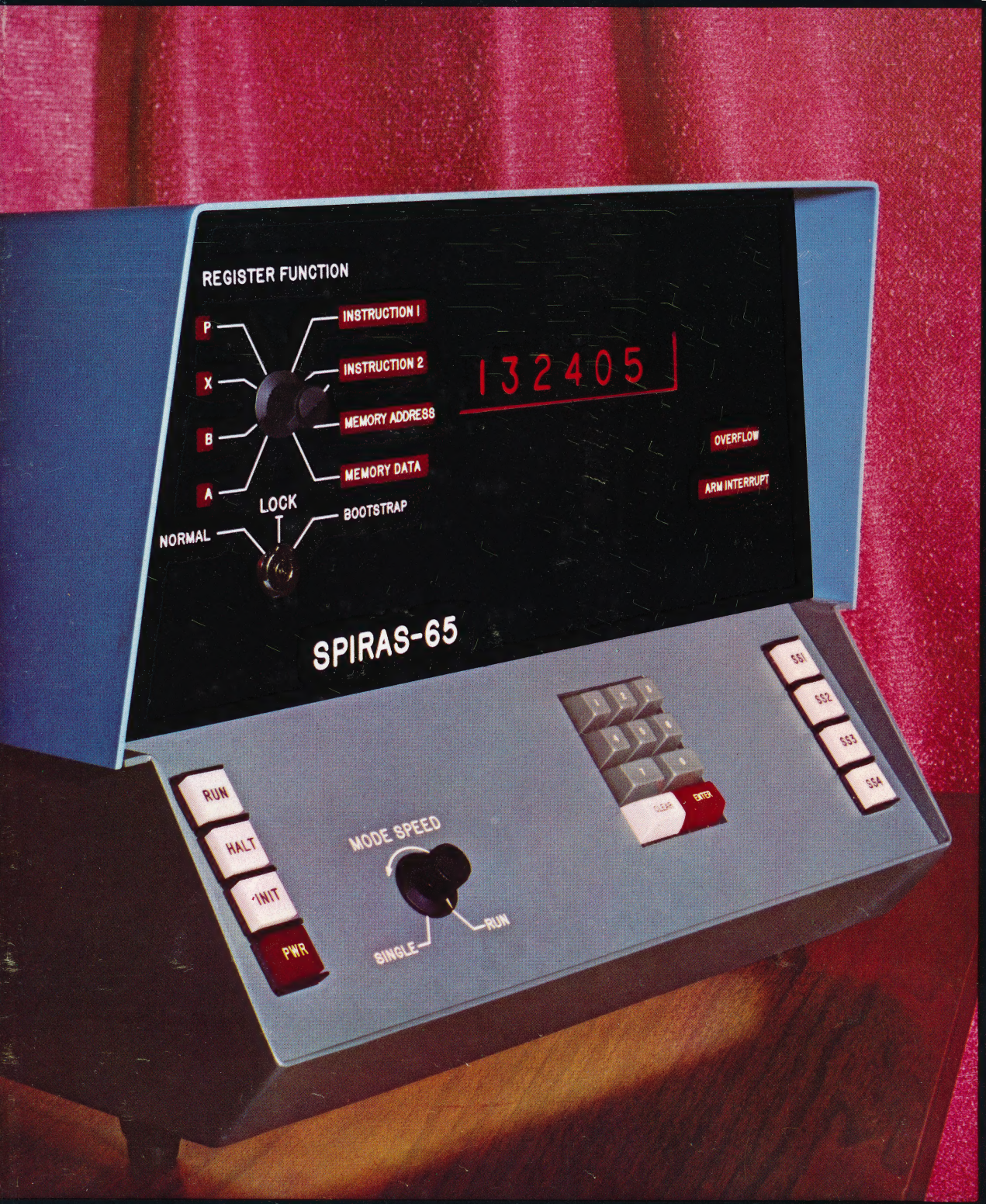
FOR SCIENCE, INDUSTRY AND BUSINESS



Spiras Systems, Inc.
Affiliate of
USM Corporation

SPIRAS-65 A STORED PROGRAM

SPIRAS-65 is a General Purpose Stored Program Controller/Processor expandable to 65 K of memory, representing unprecedented PER—FORMANCE PER DOLLAR.

SPIRAS-65 may be efficiently applied as a Data Processor or Real-Time Controller in either a dedicated and/or satellite environment.

FOR

- Industrial/Manufacturing Processes
- Numerical Machine Tools
- Data Acquisition and Analysis
- Automatic Test and Instrumentation
- Function Generation
- CRT Display Graphics Generation
- Communications Data Concentration and Distribution
- Scientific Data Processing
- Business Data Processing

ITS CREATOR

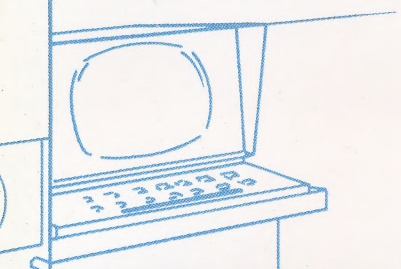
To understand the product you should know about its creator, about our fresh overview philosophy and system experience, our unique combination of talent, our total customer-service attitude, and why we designed the SPIRAS-65 to meet your needs.

Among the important commandments in our philosophy are:

- Communicate honestly and directly with the user in his own language without buzz words.
- Offer the total solution to the problem in terms of hardware and software, standard and custom.
- Provide supporting consultation, training, maintenance and a life line of information flow after the sale.

After a broad experience with available "mini-computers", we concluded that we could indeed offer dramatically improved utility, reliability and value. The approach was apparent - Build one machine without major options which includes as standard all of the performance characteristics afforded by the eclectic state of the art and realize the economy derived from large volume "one of a kind" production.

CONTROLLER/PROCESSOR



ARCHITECTURE - NVP

The SPIRAS-65 commits to hardware the IDEAL instruction repertoire to solve the broadest base system problems. The design utilizes NVP "non-volatile program" which is, in essence, a computer controlling a computer. This multigeneration system architecture also allows for customized instruction sets tailored to specific applications. NVP is a 512-word Read-Only-Memory, 32 bits long and expandable to 1024 words.

MAN/MACHINE

The SPIRAS-65 control panel is an I/O device allowing 90% of the main frame to be easily checked out by an operator. All register information is displayed on NIXIE® tubes in octal, decimal, or engineering units under program control. The data entry is via a NORMAL-WAY electronic keyset.

INDUSTRIAL DESIGN

Small LOW INERTIA circuit boards are used to reduce susceptibility to shock and vibration and minimize cost of spares.

EVALUATION

A Measurement of Computer Power - can only be made on a per application basis in terms of STORAGE/TIME/DOLLAR economy by evaluating the:

Instruction Set —
Index & Addressing Modes —
Input/Output Modes —
Software — Reliability —
Human Interface — Training —
Maintenance — Systems Support —

The specifications listed are STANDARD.

SPECIFICATIONS

GENERAL
- 16 Bit Parallel Binary
- Two's Complement Arithmetic
- Four Hardware Registers For Programmers Use
  - A Accumulator
  - B Extended Accumulator
  - X Index
  - P Program Counter

HARDWARE FUNCTIONS

Bootstrap Loader	
Add/Subtract	3.6 μsec
Multiply	17. μsec
Divide	30. μsec
Normalize	
Double Precision Add	9.0 μsec
Double Precision Subtract	10.8 μsec
Floating Point Add, Subtract, Multiply, Divide	
Priority Interrupt	
Block Transfer Cycle Stealing I/O	
Extensive Conditional Instructions	

ADDRESSING MODES

Indexing with A and X Registers	
Direct Addressing to	65 K
Relative Addressing with P Register	±511
Multilevel Indirect Addressing up to	32 K
Immediate Operations	

MEMORY

4096 to 65,536 words of Ferrite Core	
Cycle Time	1.8 μsec

INPUT/OUTPUT CHARACTERISTICS

UP TO 64 DEVICE CHANNELS
16 BIT TRANSFER

PARTY LINE - Parallel or buffered parallel	100 KC
DIRECT MEMORY CHANNEL (Block Transfer)	100 KC
DIRECT MEMORY ACCESS	500 KC

CONTROL/INDICATOR PANEL (REMOTABLE I/O DEVICE)
- DISPLAY (NIXIE) - Four Registers, Instruction Words Memory, Memory Address (in Octal, Decimal or under Program Control)
- CONSOLE STATUS INDICATOR
- DATA ENTRY - Octal Keyset
- PROGRAM SENSE - 4 Push Buttons
- MODE SWITCHES - Variable Speed

CONSTRUCTION
- MAIN FRAME COMPLEMENT: CPU with 21 IC/MSI
- GLASS EPOXY BOARDS: Up to 8K of core memory, 3 external device controllers, 10 channel I/O Bus, NVP Power Supply

LOGIC LEVELS
- DTL/TTL - 0 Volts, +5 Volts (0 Volts +3.5 Volts on I/O Busses)

DIMENSIONS
- Rack Mount with Slides 14" H x 19" W x 23" D
- Desk Top - 14" H x 19" W x 25" D

WEIGHT - 100 Pounds
HUMIDITY - 0 to 95% Relative
TEMPERATURE 10°C to 35°C
SOFTWARE
See Price List and "Excellence in Software"

PERIPHERALS
INTERFACES
OPTIONS
} See Price List

ADDRESSING

A1

XXX	a(D)	e = a	[a = 0 → 65535]
XXX*	a	a = (a)	
XXX	a(X)	e = a + (X)	
XXX*	a(X)	e = (a + (X))	
XXX*	a(Y)	e = (a) + (X)	
XXX	a(A)	e = a + (A)	
XXX	a(P)	e = a + (P)	
XXXI	a	operand = a	

A2

XXX	a(D)	e = a	[a = 0 → 65535]
XXX*	a	e = (a)	[a = 0 → 65535]
XXX	a(X)	e = a + (X)	[a = 0 → 65535]
XXX*	a(Y)	e = (a) + (X)	[a = 0 → 65535]

A3

XXXS	a(D)	e = a	[a = 0 → 1023]
XXXS*	a	e = (a)	[a = 0 → 1023]
XXXS	a(X)	e = a + (X)	[a = 0 → 1023]
XXXS	a(P)	e = a + (P)	[a = -512 → +511]

SPIRAS-65 INSTRUCTIONS

$$\text{CHP (Computer Horsepower)} = \frac{\text{Work}}{\text{Instruction}} \times \frac{\text{Instruction}}{\text{Second}}$$

$\frac{\text{Work}}{\text{Instruction}}$ is determined by:
- Size and organization of instruction set
- Flexibility of addressing and indexing modes
- Input/output structure

SPIRAS-65 offers the highest CHP per dollar in the industry.

LOAD/STORE

MNEMONIC		DESCRIPTION	TIMING
LDA	a1	(e)→(A)	[3]
LDAS	a2		[2]
LDB	a1	(e)→(B)	[3]
LDBS	a2		[2]
LDX	a1	(e)→(X)	[3]
LDXS	a2		[2]
STA	a1	(A)→(e)	[3]
STAS	a2		[2]
STB	a1	(B)→(e)	[3]
STBS	a2		[2]
STX	a1	(X)→(e)	[3]
STXS	a2		[2]
DLD	a1	(e), (e+1)→(A), (B)	[4]
DST	a1	(A), (B)→(e), (e+1)	[5]
LEA	a1	e→(X)	[4]

ARITHMETIC

MNEMONIC		DESCRIPTION	TIMING
ADD	a1	(A)+(e)→(A)	[3]
ADDS	a2		[2]
ADB	a1	(B)+(e)→(B)	[3]
ADX	a1	(X)+(e)→(X)	[3]
SUB	a1	(A)−(e)→(A)	[3]
SUBS	a2		[2]
MUL	a1	(B) * (e)→(A), (B)	[11]
MULS	a2		[10]
DIV	a1	(A), (B)/e→(B), rem→(A)	[15]
DADD	a1	(A), (B) ++(e), (e+1)→(A), (B)	[5]
DSUB	a1	(A), (B) −−(e), (e+1)→(A), (B)	[6]
FADD	a1	(A), (B).+(e), (e+1)→(A), (B)	[11-28]
FSUB	a1	(A), (B).−(e), (e+1)→(A), (B)	[11-28]
FMUL	a1	(A), (B).*(e), (e+1)→(A), (B)	[60-70]
FDIV	a1	(A), (B)./(e), (e+1)→(A), (B)	[60-70]
INR	a1	(e)+1→(e)	[4]
DCR	a1	(e)−1→(e)	[4]

SKIP INSTRUCTIONS

MNEMONIC		DESCRIPTION	TIMING
SKIP		unconditionally skip 1 word	[1]
SAZ		skip 1 word if (A) = 0	[1]
SANZ		skip 1 word if (A) ≠ 0	[1]
SAN		skip 1 word if (A) < 0	[1]
SANN		skip 1 word if (A) ≥ 0	[1]
SAP		skip 1 word if (A) > 0	[1]
SANP		skip 1 word if (A) ≤ 0	[1]
SBZ		skip 1 word if (B) = 0	[1]
SBNZ		skip 1 word if (B) ≠ 0	[1]
SXZ		skip 1 word if (X) = 0	[1]
SXNZ		skip 1 word if (X) ≠ 0	[1]
SOF		skip 1 word if (OV) = 0	[1]
SNOF		skip 1 word if (OV) ≠ 0	[1]
SS1		skip 1 word if SS1 on	[1]
SNS1		skip 1 word if SS1 off	[1]
SS2		skip 1 word if SS2 on	[1]
SNS2		skip 1 word if SS2 off	[1]
SS3		skip 1 word if SS3 on	[1]
SNS3		skip 1 word if SS3 off	[1]
SS4		skip 1 word if SS4 on	[1]
SNS4		skip 1 word if SS4 off	[1]
SKT	n	skip 1 word if any conditions True	[1]
SKF	n	skip 1 word if all conditions False	[1]
CAS	a1	IF(R) < (e), don't skip	[3]
CBS	a1	IF(R) = (e), skip 1 word	[3]
CXS	a1	IF(R) > (e), skip 2 words	[3]
DRS	a1	(e) − 1 → (e), skip if (e) = 0	[4]
IXS	n	(X) = (X)+n, skip if (X) = 0 [n=0→511]	[2]
DXS	n	(X) = (X)−n, skip if (X) = 0 [n=0→511]	[2]

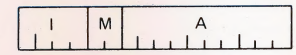
JUMP/CALL INSTRUCTIONS

MNEMONIC		DESCRIPTION	TIMING
JMP	a1	(e)→(P)	[3]
JMPS	a2	(e)→(P)	[2]
CALL	a1	*+2→e, e+1→(P)	[3]
CALS	a2	*+1→e, e+1→(P)	[2]

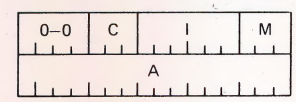
LOGICAL/CONTROL

MNEMONIC		DESCRIPTION	TIMING
AND	a1	(e) and (A)→(A)	[3]
ANDS	a2		[2]
XOR	a1	(e) eor (A)→(A)	[3]
XORS	a2		[2]
ORA	a1	(e) or (A)→(A)	[3]
ORAS	a2		[2]
HLT		Halt	[−]
NOP		No operation	[1.4]
OVF		n→OV,	[1]
SPF		1→Protect Flag	[1]

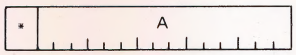
DATA WORD FORMATS



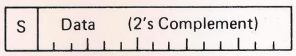
1-Word instruction



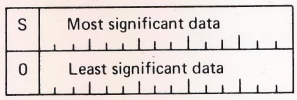
2-Word instruction



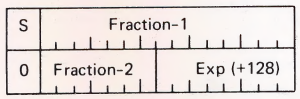
Indirect Address



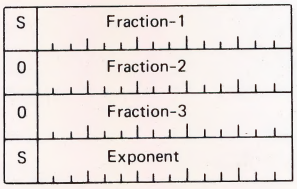
Single Precision



Double Precision

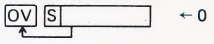
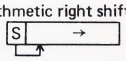
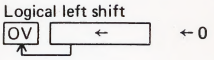
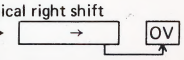
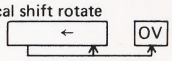
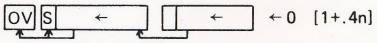
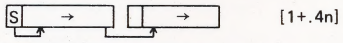
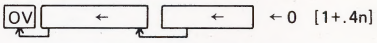
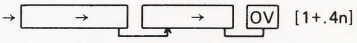
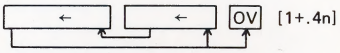


Floating Point



Double Precision Floating Point

REGISTER SHIFTING

MNEMONIC		DESCRIPTION	TIMING
ASLA	n	Arithmetic left shift	[1+.2n]
ASLB	n		
ASRA	n	Arithmetic right shift	[1+.2n]
ASRB	n		
LSLA	n	Logical left shift	[1+.2n]
LSLB	n		
LSRA	n	Logical right shift	[1+.2n]
LSRB	n		
LRLA	n	Logical shift rotate	[1+.2n]
LRLB	n		
ASLD	n		[1+.4n]
ASRD	n		[1+.4n]
LSLD	n		[1+.4n]
LSRD	n		[1+.4n]
LRLD	n		[1+.4n]

REGISTER TRANSFER

MNEMONIC					TIMING
CP	s,d	[CPF]	(s)→(d)	[if OV=1]	[1.4]
CPI	s,d	[CPIF]	(s)+1→(d)	[if OV=1]	[1.4]
CPD	s,d	[CPDF]	(s)−1→(d)	[if OV=1]	[1.4]
CPC	s,d	[CPCF]	($\bar{s}$)→(d)	[if OV=1]	[1.4]
CPN	s,d	[CPNF]	-(s)→(d)	[if OV=1]	[1.4]
CAB	s,d	[CABF]	(A)→(B), (s)→(d)	[if OV=1]	[1.4]
CAX	s,d	[CAXF]	(A)→(X), (s)→(d)	[if OV=1]	[1.4]
CXB	s,d	[CXBF]	(X)→(B), (s)→(d)	[if OV=1]	[1.4]
RGC	nnn	Operation depends on bits nnn			[1.4]

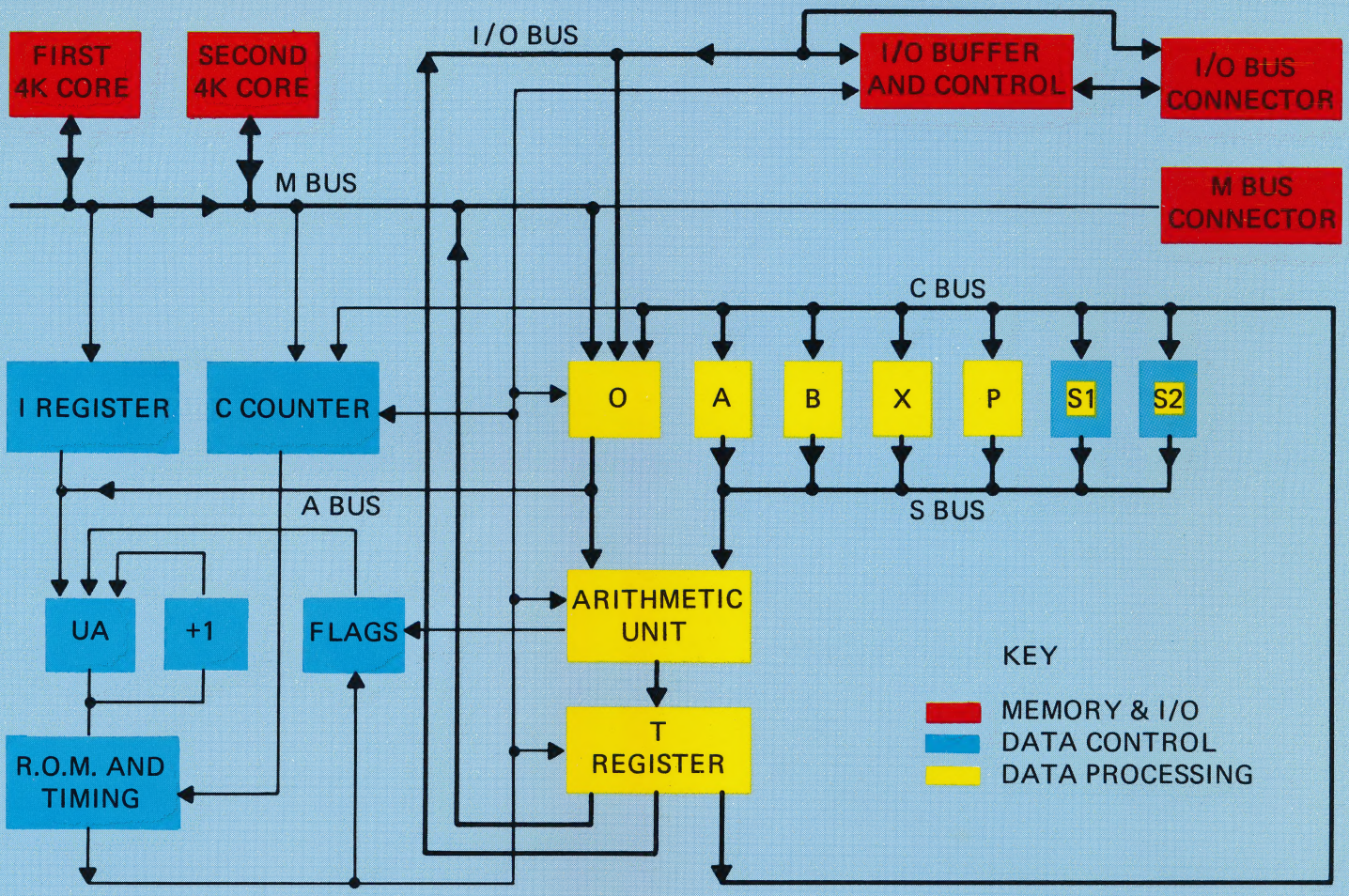
s = Zero, A, B or X
d = Zero, A, B, X, AB, AX, BX or ABX

OUTPUT

MNEMONIC		DESCRIPTION	TIMING
EXCA	n	(A) → device n control	[1]
EXCB	n	(B) → device n control	[1]
EXCX	n	(X) → device n control	[1]
EXCM	n,a3	(e) → device n control	[3]
EXCI	n,v	v → device n control	[2]
OTA	n	(A) → device n data	[1]
OTB	n	(B) → device n data	[1]
OTX	n	(X) → device n data	[1]
OTM	n,a3	(e) → device n data	[2]
OTI	n,v	v → device n data	[3]
ARM		arm interrupts, 0 → OV	[1]
DRM		disarm interrupts, 0 → OV	[1]
ARMF		arm interrupts, 1 → OV	[1]
DRMF		disarm interrupts, 1 → OV	[1]

INPUT

MNEMONIC		DESCRIPTION	TIMING
SENA	n	device n status → (A)	[1]
SENB	n	device n status → (B)	[1]
SENX	n	device n status → (X)	[1]
SENM	n,a3	device n status → (e)	[3]
SENS	n,m	skip if device n status (masked by m) = 0	[2]
CIA	n	device n data → (A)	[1]
CIB	n	device n data → (B)	[1]
CIX	n	device n data → (X)	[1]
CIM	n,a3	device n data → (e)	[3]
INA	n	device n data OR (A) → (A)	[1]
INB	n	device n data OR (B) → (B)	[1]
INX	n	device n data OR (X) → (X)	[1]



SPIRAS-65 BLOCK DIAGRAM

excellence in software

We can provide complete systems to the customer because of the extensive software package offered with each SPIRAS-65 unit. In addition to the programs described below, our staff of engineers and programmers can provide applications programs to fit customer requirements.

SYMBOLIC MACRO ASSEMBLER PROGRAM

Free format input.

Macro capability with noise words allowed in the argument list (8K required).

Listing includes octal value generated, relative assignment address, sequential line number, detailed error diagnostics, and a symbol table cross-reference listing (concordance).

Listing control pseudo-ops provided.

Absolute or relocatable object output fully compatible with FORTRAN object output.

System provides capability for sharing literals between sub-programs, and allows page-free addressing (system creates indirect address links automatically if needed).

Operates in as little as 4K of memory (no macros).

FULL ASA FORTRAN-IV COMPILER

Operates in one pass in as little as 8K of memory.

High level of expression, subscript and register optimization.

I/O device independent.

Comprehensive error diagnostic logic.

Symbolic output listing provided with side-by-side octal output data.

Relocatable object output, fully compatible with assembly output.

(continued)

EXCELLENCE IN SOFTWARE

LINKING LOADER PROGRAM

Loads absolute or relocatable programs.
Device independent operation.
Provides memory map.
Manages literal and indirect pointer pool.
Generates indirect addresses, if required.
Searches library tapes, if necessary.

DEBUG PROGRAM

Type memory in octal.
Memory modifications in octal.
Display and modify live registers.
Masked memory search within limits.
Enter break point and start compute.
Makes self loading tapes.

SOURCE PROGRAM EDITOR

Permits modification of source tapes (or disks).
Insertions and deletions by line number.

OBJECT PROGRAM EDITOR

Subroutines can be inserted, deleted or replaced in library tapes (or from disk).

INPUT/OUTPUT LIBRARY

ASCII to/from Binary Conversion
- Fixed point single precision.
- Fixed point double precision.
- Floating point single precision.
- Floating point double precision.
- Integer.

Device Drivers for All I/O Devices
- Open device.
- Read/write data record.
- Close-out device.
- Provide special I/O function.

MATH LIBRARY

Single precision fixed point functions.
Double precision fixed point functions.
Single precision floating point functions.
Double precision floating point functions.
Complex functions.
Complete FORTRAN IV function library.

DIAGNOSTICS

CPU diagnostic.
Memory diagnostic.
Peripheral test programs.

OPERATING SYSTEM

Allows operator assignment of I/O devices.
Controls loading and operating of programs in batch mode.
Operates with basic computer system, a mag-tape system, or with a disk system.

CONVERSATION LANGUAGE*

Includes BASIC as a subset.
Allows macros to be defined and called.
Free-format including noise words and macros allows custom, user-oriented "languages" to be easily generated and used.

360-ASSEMBLER*

Allows assembly of SPIRAS-65 programs on the IBM-360 computer (Model 30 and above).
Available also on most other large computers.
Object output compatible with SPIRAS-65 assembly program object output.

360-SIMULATOR*

Allows simulation of SPIRAS-65 programs on the IBM computer (Model 30 and above).
Detailed trace listings and memory dumps available.
Available also on most other large computers.

*May be purchased. Not included with standard soft ware package.

SPIRAS-65 has a twin called the IRASCOPE which is a DATA BASE EDITING DISPLAY.

Consider it as a peripheral to your SPIRAS-65.

Spiras Systems, Inc.
affiliate of
USM Corporation

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Waltham, Massachusetts 02154
617-891-7300 TWX 710-324-6699

USM is a world-wide 400 million dollar designer and manufacturer of systems, aimed at improving the productivity of manufacturing and service industries.

Spiras Systems Inc.,
formerly I.R.A. Systems, Inc.